1. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a passivation layer disposed upon said upper surface, said passivation layer comprising ammonia or derivatives thereof adsorbed upon said upper surface; and

an interlayer dielectric disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface.

7. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect having an upper surface and being disposed within a dielectric layer, said electrically conductive interconnect including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a first passivation layer comprising a tungsten nitride compound and being disposed upon said upper surface;

a second passivation layer comprising ammonia or derivatives thereof adsorbed upon said first passivation layer; and

an interlayer dielectric disposed upon said dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface.

8. (Once Amended) A semiconductor structure comprising:

an electrically conductive interconnect disposed within a dielectric layer, said electrically conductive interconnect having an upper surface and including:

a titanium liner layer disposed within a depression in said dielectric layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer and filling said depression;

a passivation layer disposed upon said upper surface comprising ammonia or derivatives thereof adsorbed upon said upper surface; and

an interlayer dielectric disposed upon said dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface.

9. (Once Amended) An interconnect in an electronic device comprising:

a metallic first structure disposed within a first silicon oxide layer, said metallic first structure having an upper surface;

a passivation layer disposed upon said upper surface, said passivation layer comprising ammonia or derivatives thereof adsorbed upon said upper surface; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

10. (Once Amended) An interconnect in an electronic device according to Claim 9, wherein said metallic first structure further comprises:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer.

15. (Once Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a first passivation layer disposed upon said upper surface and comprised of a tungsten nitride compound;

a second layer comprising ammonia or derivatives thereof adsorbed upon said first passivation layer; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

16. (Once Amended) An interconnect in an electronic device comprising:

a metallic structure disposed within a first silicon oxide layer, said metallic structure having an upper surface and including:

a titanium liner layer disposed within an interconnect corridor in said first silicon oxide layer;

a titanium nitride layer disposed upon said titanium liner layer; and

a tungsten film disposed upon said titanium nitride layer;

a passivation layer disposed upon said upper surface and comprised of ammonia or derivatives thereof adsorbed upon said upper surface; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

Please add the following new claims:

17. A semiconductor structure comprising:

an electrically conductive interconnect disposed within a first dielectric layer, said electrically conductive interconnect having an upper surface;

a first passivation layer disposed upon said upper surface, said first passivation layer comprising a tungsten nitride compound;

a second passivation layer adsorbed upon said first passivation layer, said second passivation layer comprising ammonia or derivatives thereof; and

an interlayer dielectric disposed upon said first dielectric layer and upon said upper surface, said interlayer dielectric being continuously adhered to said upper surface.

18. A semiconductor structure according to claim 17, wherein said first passivation layer has a thickness of less than about 50 Å.

19. An interconnect in an electronic device comprising:

a metallic first structure disposed within a first silicon oxide layer, said metallic first structure having an upper surface;

a first passivation layer disposed upon said upper surface, said first passivation layer comprising a tungsten nitride compound;

a second layer adsorbed upon said first passivation layer, said second layer comprising ammonia or derivatives thereof; and

a second silicon oxide layer disposed upon said first silicon oxide layer and upon said upper surface, said second silicon oxide layer being continuously adhered to said upper surface.

20. An interconnect according to claim 19, wherein said first passivation layer has a thickness of less than about 50 Å.

21. A semiconductor structure according to claim 1, wherein said ammonia derivative comprises nitrogen-containing silane.

22. A semiconductor structure according to claim 7, wherein said ammonia derivative comprises nitrogen-containing silane.

23. A semiconductor structure according to claim 8, wherein said ammonia derivative comprises nitrogen-containing silane.

24. An interconnect according to claim 9, wherein said ammonia derivative comprises nitrogen-containing silane.

25. An interconnect according to claim 15, wherein said ammonia derivative comprises nitrogen-containing silane.

26. An interconnect according to claim 16, wherein said ammonia derivative comprises nitrogen-containing silane.

27. A semiconductor structure according to claim 17, wherein said ammonia derivative comprises nitrogen-containing silane.

28. An interconnect according to claim 19, wherein said ammonia derivative comprises nitrogen-containing silane.